ABSTRACT

A PLL frequency synthesizer is provided that enables improvement of near C/N, shortening of lockup time, and reduction of residual FM to be achieved. In this apparatus, phase comparison is performed by a phase comparator (101) on a signal input from an input terminal I1 and a signal output from a frequency divider (107), and a current signal corresponding to the phase difference is converted to a voltage signal by one of a plurality of loop filters (103 or 104) with different cutoff frequencies, and is output to a voltage controlled oscillator (106). The output to a voltage controlled oscillator (106) generates a frequency signal corresponding to the input voltage signal. The oscillation signal is branched at junction point P1, and is output to the frequency divider (107) and output terminal O1. A variable capacitance capacitor (108) is connected to junction point P2 further branching subsequent to junction point P1 and its capacitance is controlled in accordance with loop filter switching control by a control circuit (109).